AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph starting on page 8, line 24 with the following paragraph:

The circuit 100 generally comprises a circuit 110 and a circuit 112. In one example, the circuit 110 ~~maybe~~ may be a vertical filter circuit. The circuit 112 may be a horizontal filter circuit. The circuit 110 may have an input that may receive the signal DATA[63:0], an input/output that may receive/present the signals ACCESSa-ACCESSn, and an output that may present one or more signals (e.g., DOUT0-DOUT3). The circuit 110 may be serially coupled to the circuit 112. The signals DOUT0-DOUT3 may be vertically scaled pixels (pels) that may be presented to an input of the horizontal filter 112. The circuit 112 may have an input/output that may receive/present the signals ACCESSa-ACCESSn and an output that may present the signal PD[7:0].

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Please replace the paragraph starting on page 14, line 1 with the following paragraph:

Referring to FIG. 11, a block diagram 200 of hierarchy of the address generator circuit 140 is shown. The address generator circuit 140 generally provides an interface to read data from the SDRAM. The module 200 may be subdivided into the main finite state machine (FSM) controls for luma (e.g., block 220), for chroma

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(e.g., block 222), a segment allocator (e.g., block 224), and additional control (e.g., block 226). A segment allocator block similar to the circuit 224 is configured to implement a reduced memory mode (e.g., 2.5 times frame decoding) in the conventional design.

Please replace the paragraph starting on page 15, line 27 with the following paragraph:

Some of the FSM 220 states may be common ~~will~~ to all of the display modes of the circuit 100. However, a section of the FSM 220 may have modifications in a state (e.g., MAIN_VPS_INIT) to select the line address increment in a signal (e.g., L_PEL_SEL) for the new modes 12 and 13. In an initial state (e.g., MAIN_INIT3) the signal L_PEL_SEL may also increment by one line when displaying the bottom field of an interlaced picture in mode 13. The state MAIN_INIT3 may then move to the linestore preload. The linestore preload may be common with the existing mode 3 and 8 section of the FSM 220.